**EXPERIMENT 03**

**Implementation of Basic Gates using Universal Gates**

**Objectives:**

Using two input NAND and NOR gates, construct the following

1. NOT
2. AND
3. OR

After doing this, implement the given expression on the trainer board.

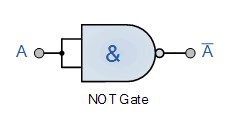
**Equipment /Tool:**

Trainer, IC 74LS00, 74LS02.

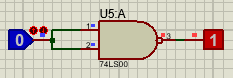
**Theory:**

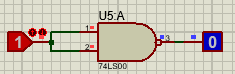
NAND and NOR gates are called universal gates because we can make any basic gate from them by using the following circuits.

* 1. **Implementation of Gates using NAND Gate only: i) NOT Gate Behavior:**

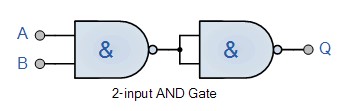


|  |  |
| --- | --- |
| **Input** | **output** |
| 0 | 1 |
| 1 | 0 |

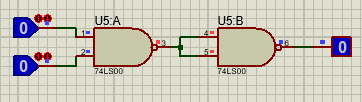


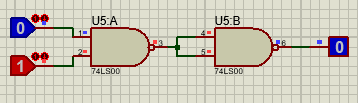


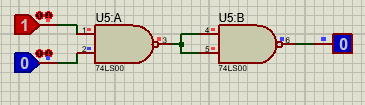
* 1. **AND Gate Behavior:**

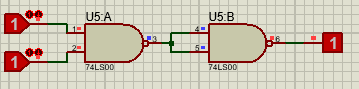


|  |  |  |
| --- | --- | --- |
|  | **Input** | **Output** |
| A | B | Q |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

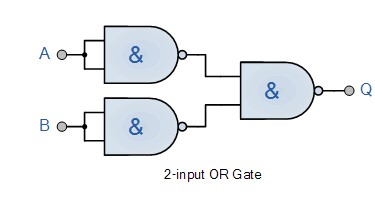




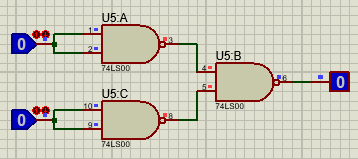


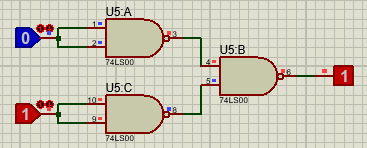


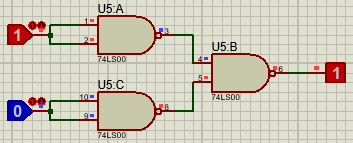
* 1. **OR Gate Behavior:**

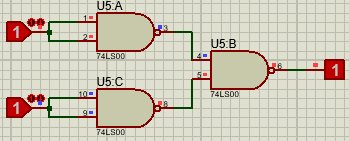


|  |  |  |
| --- | --- | --- |
|  | **Input** | **Output** |
| X | Y | F |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |





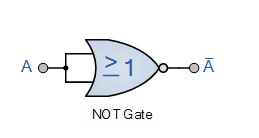




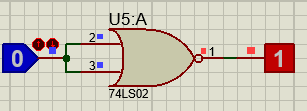
* 1. **Implementation of Gates using NOR Gate Only:**

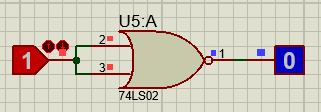
Verify all the truth tables for all the gates.

**i) NOT Gate Behavior:**

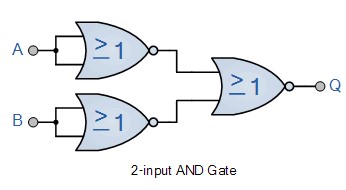


|  |  |
| --- | --- |
| **A** | **A’** |
| 0 | 1 |
| 1 | 0 |

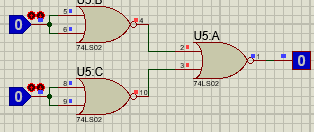
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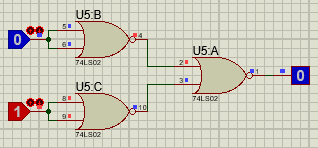
****

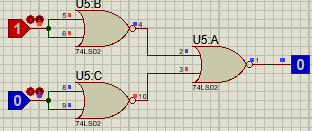
**ii) AND Gate Behavior:**

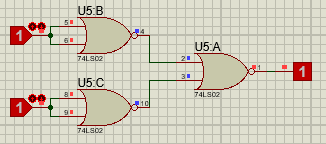


|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Q** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

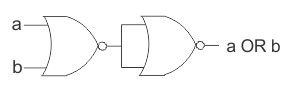




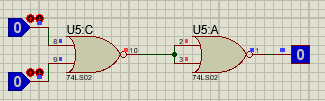


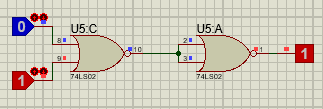


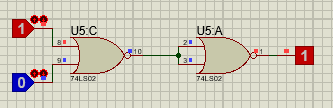
**iii) OR Gate Behavior:**

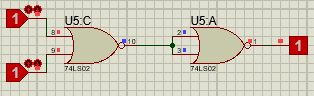


|  |  |  |
| --- | --- | --- |
| **A** | **B** | **F** |
| 0 | 0 | 0 |
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |









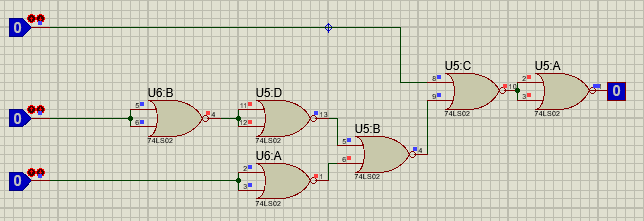
**Exercise in Lab:**

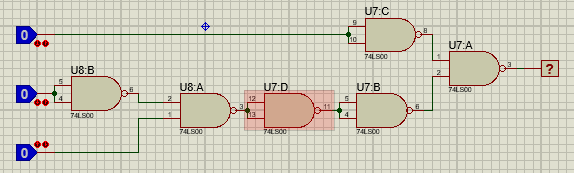
* 1. Implement following expression using NOR Gate only.
  2. Implement following expression using NAND Gate only.

**F=**𝑿 + 𝒀. 𝒁

**Circuit diagram**

1)





**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Input** |  | **Output** |
| **X** | **Y** | **Z** | **F** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

